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In the Specification:

- [29] The BIST sequence controller is coupled to control line-40-44 for providing control signals to the SERDES circuits to enable the SERDESs and set the loop mode, for example. The BIST sequence controller also provides the error detection signal over line 46.
- [32] As previously mentioned, the programmable transmit register generates and transmits programmably varying data patterns to the SERDES circuits. The SERDES circuits process the transmitted data into processed data and returns the processed data to the receive register 54 over the receive bus 44. The comparator-42–52 then compares the processed data received by the received register 54 to the transmitted data transmitted by the transmit register 56. Should the comparator 52 detect any errors between the processed and transmitted data, the BIST sequence controller 50 will issue an error signal over the error detected line 46.
- The various data patterns may be accessed and programmed serially through scan chain inputs 118. Alternatively, this may be accomplished in parallel through internal busses—120_122 or control signals—122_120. Either serial scan chain or parallel bus signals requires a clock (not shown) as will be understood by those skilled in the art. In practice, a parallel interface would operate at higher speed than a scan chain interface, and would be more practical for invoking the register array words.